REMARKS

The Official Action dated March 23, 2005 has been received and its contents carefully noted. In view thereof, claims 1, 21, 25, 26, 27 and 29 have been amended in order to better define that which Applicant regards as the invention. As previously, claims 1-29 are presently pending in the instant application with claims 6-20 being withdrawn from further consideration by the Examiner as being directed to a non-elected invention.

With reference now to the Official Action and particularly page 2 thereof, Applicant hereby confirms the election of Species I, drawn to Fig. 1 with claims 1-5 and 21-29 being readable thereon. In view of the foregoing amendments, it is respectfully submitted that each of claims 1-5 and 21-29 are now in proper condition for allowance.

With reference to paragraph 2 of the Office Action, claims 21, 25, 27 and 29 have been objected to as including minor informalities. As can be seen from the foregoing amendments, each of claims 21, 25, 27 and 29 have been amended as suggested by the Examiner. Accordingly, each of these claims are now believed to be proper formal condition for allowance.

With reference now to paragraph 4 of the Office Action, claims 1, 3-5, 21, 23-26, 28 and 29 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art ("Admission") in view of U.S. Patent No. 6,037,792 issued to McClure. This rejection is respectfully traversed in that the combination proposed by the Examiner neither discloses nor suggests that which is presently set forth by Applicant's claimed invention.

Applicant's claimed invention as recited in independent claim 1, as amended, is directed to a nonvolatile semiconductor memory device comprising a memory cell array having a plurality of memory cells and arranged in an array, the memory cells being

connected to a plurality of bit lines and word lines, a plurality of address input terminals inputting a plurality of addresses thereto, a test mode circuit for outputting a test mode signal when a signal is inputted to a predetermined terminal among the address input terminals, a row decoder connected to the test mode circuit and applying an excess voltage for a test to all the word lines in response to the test mode signal, a column decoder connected to the test mode circuit and setting all the bit lines to a non-selecting state in response to the test mode signal and a monitor terminal connected to the test mode circuit for outputting the test mode signal. Similarly, independent claim 21 is directed to a semiconductor memory device comprising a memory cell array having a plurality of memory cells, a plurality of word lines and a plurality of bit lines. A plurality of address input terminals for receiving a plurality of address signals is provided as well as a test mode circuit connected to the address input terminals, the test mode circuit providing a test mode signal in response to the address signals received thereto. Also provided is a row decoder connected to the test mode circuit and the memory cell array, the row decoder applying an excess voltage to all of the word lines in response to the test mode signal, a column decoder connected to the test mode circuit and the memory cell array, and a monitor terminal connected to the test mode circuit for outputting the test mode signal.

Independent claim 26 similarly recites a semiconductor memory device comprising a memory cell array having a plurality of memory cells, plurality of word lines and a plurality of bit lines, a plurality of address input terminals for receiving a plurality of address signals, a test mode circuit connected to the address input terminals, the test mode circuit providing a test mode signal in response to the address signals received thereto, a row decoder connected to the test mode circuit and the memory cell array, the row decoder applying an excess voltage to all of the word lines in response to the test mode signal, a column decoder

connected to the test mode circuit and the memory cell, the column decoder receiving the test mode signal and a monitor pad connected to the test mode circuit for outputting the test mode signal. It is respectfully submitted that the combination proposed by the Examiner fails to disclose or suggest those features recited in each of independent claims 1, 21 and 26.

As noted hereinabove, the present invention relates to a semiconductor memory device having a monitor terminal for outputting a test signal. The test signal places the semiconductor memory device in a test mode. In this test mode, an excess voltage is applied to all of the word lines in response to the test mode signal. This test confirms defective memory cells and removes such defective memory cells as is set forth in Applicant's specification at page 6, line 25 through page 7, line 13. Furthermore, in accordance with Applicant's claimed invention the test mode is monitored by the monitoring pad as noted from Applicant's specification at page 7, line 14 through page 8, line 13.

In rejecting Applicant's claimed invention, the Examiner states that since it was common and well known in the art to detect a predetermined signal on an existing address pin to enable a test mode, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to enable the test mode of Applicant's admission by way of a signal on a predetermined terminal among the address input terminals, for the purpose of reducing the need for additional pins to enable a test mode and thus reducing the space and costs associated with providing additional pins. In this regard, it is noted that McClure discloses a semiconductor memory device having a flag terminal for outputting a burn-in stress test signal. The burn-in stress test is conducted at significantly higher voltages and temperature conditions in order accelerate weak bit failures and infant life failures as noted in column 3, lines 7-10. Furthermore, the burn-in stress test is conducted in a burn-in oven as noted from the Abstract. Accordingly, the flag terminal of McClure is used for

confirming whether the device is in the burn-in stress mode or not. Clearly, the flag pad of McClure and the monitoring pad of the present invention are significantly different. Consequently, it is respectfully submitted that one of ordinary skill in the art would not modify the admitted prior art in the manner suggested by the Examiner. Moreover, even if modified in the manner suggested by the Examiner, Applicant's claimed invention as set forth in each of independent claims 1, 21 and 26 is clearly not achieved. Therefore, in view of the foregoing it is respectfully submitted that Applicant's claimed invention as set forth in each of independent claims 1, 21 and 26 clearly distinguish over the combination proposed by the Examiner and are in proper condition for allowance.

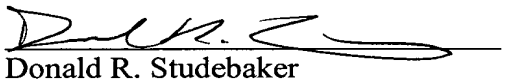
With reference to paragraph 5 of the Office Action, claims 2, 22 and 27 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Applicant's admitted prior art in view of McClure as applied to claims 1, 21 and 26 and further in view of U.S. Patent No. 5,982,677 issued to Fontana et al. This rejection is likewise respectfully traversed in that the patent to Fontana et al. does nothing to overcome the aforementioned shortcomings associated with the prior art combination.

While the patent to Fontana et al. may disclose a select line connected to the drain of a memory cell, and a regulator connected to the select line, as noted hereinabove, Fontana et al. fails to overcome the aforementioned shortcomings associated with the teachings of McClure. Accordingly, in that each of claims 2, 22 and 27 are directly dependent upon independent claims 1, 21 and 26 respectively, and include all the limitations thereof, it is respectfully submitted that Applicant's claimed invention as set forth in each of these claims is likewise in proper condition for allowance for the reasons discussed hereinabove.

Therefore, in view of the foregoing it is respectfully requested that the objections and rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-5 and 21-29 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



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